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EXAMINER	
MOON, SEOKYUN	

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2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,776	KIM ET AL.	
	Examiner	Art Unit	
	SEOKYUN MOON	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9,11-13,15-19 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,11-13,15-19,and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The Applicant's arguments filed on August 11, 2008 have been fully considered.

The Applicant argued [Remarks: pg 8 last paragraph – pg 9 1st paragraph] that the Applicant disagrees with the obviousness of combining the prior arts of record, stated in the previous Office Action because the advantages of the instant invention are different from the advantages of the prior arts.

However, Examiner respectfully submits that the fact that the prior arts of record have advantages different from the advantages of the instant invention does not prove or explain anything regarding the obviousness of the prior arts. Additionally, those advantages are not recited in the claims.

The Applicant argued [Remarks: pg 9 2nd full paragraph] that Kudo does not teach the claim limitation.

However, Examiner respectfully submits that the combination of the references was based on the concept of modifying the device of Park using the concept of Kudo rather than incorporating the whole structure of the device of Kudo into the device of Park.

The Applicant's arguments regarding the newly added claim limitation are moot in view of new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1**, **2**, **4-6**, **8-9**, **11-13**, **15-17**, **19**, and **21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (US 2002/0015028) in view of Kudo (US 2006/0033695) and Nakano (US 7,098,901).

As to **claim 1**, Park teaches an apparatus for driving a liquid crystal display [fig. 1 and par. (0026) lines 1-3], the apparatus comprising:

a signal controller ("*controller 20*") [fig. 2 and par. (0033)] for generating image data ("*column control signal*", and "*R, G, B* data") [fig. 2 and par. (0034) line 5] for different pixel colors ("*R*, *G*, and *B*") and digital gamma signals ("*gamma data*") [par. (0034) lines 7-8] for different pixel colors;

a plurality of gray voltage generators (a combination of "*memory 32*, "*decoder 33*", and "*D/A converter 34*" included in each of the "*column driver ICs 14*") [fig. 3] receiving the digital gamma signals ("*gamma data*") that are useful for generating gamma curves for the different pixel colors ("*R*, *G*, and *B*") from the signal controller ("*controller 20*") [fig. 1] and converting the digital gamma signals into analog gamma reference voltages, the gray voltage generators including:

a first gamma voltage register (a register included in "*memory 32*") [fig. 3]; and

a plurality of data drivers (a combination of "*shift register 24*", "*data latch 26*", "*D/A converter 28*", and "*buffer 30*" included in each of the "*column driver ICs 14*") [fig. 3] coupled

to the plurality of gray voltage generators and the signal controller, wherein each of the data drivers individually receives analog gamma reference voltages and selects a gray voltage based on the analog gamma reference voltages [par. (0037), emphasis on lines 7-13];

wherein the generating of the gamma curves is done by the gray voltage generator (a combination of "*memory 32*, "*decoder 33*", and "*D/A converter 34*" included in each of the "*column driver ICs 14*") [fig. 3].

As discussed above, Park teaches the signal controller ("*controller 20*") [fig. 2] generating same digital gamma signals for same pixel colors [par. (0034) lines 7-12].

Park does not expressly teach the signal controller generating different digital gamma signals for different pixel colors.

However, Kudo teaches a concept of generating and processing different digital gamma signals for different pixel colors [par. (0107) lines 1-4 and par. (0108)].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the signal controller of Park to generate different digital gamma signals for different pixel colors by applying the concept of Kudo, i.e. generating different digital gamma signals for different pixel colors, to the apparatus of Park, and to modify the gray voltage generators of Park to produce analog gamma reference voltages that are specific to different pixel colors and are associated with the same pixel color as the image data, by including additional memory, decoder, and D/A converter, by applying the concept of Kudo, i.e. processing different digital gamma signals for different pixel colors, to the apparatus of Park, in order to allow the data drivers of Park to output data voltages representing more accurate gamma curves to the liquid crystal panel of the display and thus to improve the image quality of the display.

Park as modified by Kudo teaches the plurality of data drivers being coupled to the plurality of gray voltage generator.

Park as modified by Kudo does not expressly teach the plurality of data drivers being coupled to a single gray voltage generator.

However, Nakano teaches a concept of including a single gray voltage generator ("*1436*") [fig. 14] coupled to a plurality of data drivers ("*source drivers 1435*") [fig. 14], which provides a plurality of reference voltages to the plurality of data drivers [col. 21 lines 42-49].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the apparatus of Park as modified by Kudo to include a single external gray voltage generator, instead of including a plurality of gray voltage generators, as taught by Nakano, in order to reduce the manufacturing cost of the liquid crystal display driving apparatus.

Park as modified by Kudo and Nakano teaches a first color-specific gamma voltage register (Park: a register included in "*memory 32*") [Park: fig. 3] storing digital gamma voltages received from the signal controller for a specific color.

Park as modified by Kudo and Nakano does not teach a second color-specific gamma voltage register coupled to the first color-specific gamma voltage register wherein the second color-specific gamma voltage register stores digital gamma voltages received from the signal controller for a specific pixel color.

However, since the Applicant has failed to disclose having two color-specific gamma voltage registers instead of one color-specific gamma voltage register provides an advantage, is used for a particular purpose, or solves a state problem, it is an obvious matter of design choice to include two color-specific gamma voltage registers.

Furthermore, the courts have held that separating a single part (the color-specific gamma voltage register of Park as modified by Kudo and Nakano) into a plurality of separated parts (the first and the second color-specific gamma voltage register) is generally recognized as being within the level of ordinary skill in the art. *In re Dulberg*, 289 F.2d 522, 523, 129 USPQ 348, 349 (CCPA 1961).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use either one or two of color-specific gamma voltage registers to store digital gamma voltages received from the signal controller since either one or two of color-specific gamma voltage registers would perform equally well at storing digital gamma voltages temporarily.

As to **claim 2**, Park as modified by Kudo and Nakano teaches the gray voltage generator storing gray voltages for each of the pixel colors [Park: par. (0038)].

Park does not expressly teach the gray voltage generator separately storing gray voltages for each voltage polarity.

However, Kudo [fig. 13] further teaches a gray voltage generator storing gray voltages for each voltage polarity.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the signal controller of Park to include registers storing gray voltages for each voltage polarity and to modify the gray voltage generator of Park to generate gray voltage signals that are specific to different voltage polarities by including additional memory, decoder, and D/A converter for each voltage polarity such that the gray voltage generator of Park separately stores gray voltages for each voltage polarity, as taught by Kudo, in order to output gray voltages

representing more accurate gamma curves to the liquid crystal panel of the display of Park as modified above, and thus to improve the image quality of the display.

As to **claim 4**, Park as modified by Kudo and Nakano teaches the gray voltage generator comprising a digital-to-analog converter (Park: a combination of "*33*" and "*34*") [Park: fig. 3] for converting the digital gamma voltages that are stored in the first and the second color-specific gamma voltage registers into analog gray voltages [Park: par. (0038) lines 3-6].

As to **claim 5**, as discussed with respect to the rejection of claim 1, in the apparatus of Park as modified by Kudo and Nakano, the first color-specific gamma voltage register and the second color specific gamma voltage register are connected to each other and the second color-specific gamma voltage register is used to store the digital gamma values processed by the first color-specific gamma voltage register temporarily. Thus, the number of bits for the input of the second color-specific gamma voltage register is same as the number of bits for the output of the second color-specific gamma voltage register.

Park as modified by Kudo and Nakano does not expressly teach the buses being ten-bit buses.

However, since the Applicant has failed to disclose specifying the number of bits of the buses to be ten-bits provides an advantage, is used for a particular purpose, or solves a stated problem, it is an obvious matter of design choice to specify the number of bits of buses as being ten.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use any reasonable number of bits capable of carrying gamma data for the buses

since reasonable number of bits capable of carrying gamma data would perform equally well at transferring digital gamma data.

As to **claim 6**, Park as modified by Kudo and Nakano teaches that the data driver (Park: a combination of "*shift register 24*", "*data latch 26*", "*d/a converter 28*", and "*buffer 30*" included in a plurality of "*column driver IC 14*") [Park: figs. 1 and 3] comprises a plurality of data driving circuits for receiving image data (Park: "*column control signal*", and "*R, G, B* data") and data control signals (Park: "*scan control signal*") from the signal controller (Park: "*controller 20*") [Park: fig. 1] [Park: par. (0037)], wherein each of the data driving circuits (Park: a combination of "*shift register 24*", "*data latch 26*", "*d/a converter 28*", and "*buffer 30*") [Park: fig. 3] includes a sampling unit (Park: a combination of "*D/A converter 28*" and "*buffer 30*") for sampling gamma voltage data from the digital-to-analog converter (Park: a combination of "*33*" and "*34*").

As to **claim 8**, Park as modified by Kudo and Nakano teaches the image data being transmitted from the signal controller (Park: "*controller 20*") [Park: fig. 1] to the data driving circuits (Park: a combination of "*shift register 24*", "*data latch 26*", "*d/a converter 28*", and "*buffer 30*" included in each of a plurality of "*column driver IC 14*") [Park: figs. 1 and 3] by two signal lines [fig. 3] that are separately connected between the data driving circuits and the signal controller.

As to **claim 9**, Park as modified by Kudo and Nakano teaches the gray voltage generator (Park: a combination of "*memory 32*", "*decoder 33*", and "*D/A converter 34*" included in a plurality of "*column driver IC 14*") [Park: figs. 1 and 3] being coupled to the data driver (Park: a combination of "*shift register 24*", "*data latch 26*", "*d/a converter 28*", and "*buffer 30*" included

in a plurality of "*column driver IC 14*") [Park: figs. 1 and 3] by a plurality of buses [Park: fig. 3] (one bus for each color, as modified in the combination).

As to **claim 11**, Park as modified by Kudo and Nakano teaches a gate driver (Park: a combination of "*scan driver IC 12*") [Park: fig. 1] coupled to the signal controller (Park: "*controller 20*"), wherein the gate driver generates gate control signals in response to signals from the signal controller [Park: par. (0028) lines 7-9 and par. (0030) lines 8-9].

As to **claim 12**, Park teaches a liquid crystal panel assembly [par. (0026) lines 1-3] comprising:

a plurality of pixel electrodes (any liquid crystal display includes a plurality of pixel electrodes) wherein each of the pixel electrodes is associated with a pixel color (R, G, or B);

a liquid crystal layer [par. (0002)];

a plurality of data drivers (a combination of "*shift register 24*", "*data latch 26*", "*d/a converter 28*", and "*buffer 30*" included in a plurality of "*column driver IC 14*") [figs. 1 and 3] for supplying data signals to the pixel electrodes; and

a signal controller ("*controller 20*") [fig. 2 and par. (0033)] coupled to the data drivers (a combination of "*shift register 24*", "*data latch 26*", "*d/a converter 28*", and "*buffer 30*" included in a plurality of "*column driver IC 14*") [figs. 1 and 3], wherein the signal controller has a register for storing a predetermined number of digital gamma data that are useful for generating gamma curves ("*gamma data*") [par. (0034) lines 7-8] for different pixel colors ("*R*, *G*, and *B*");

a plurality of gray voltage generators (a combination of "*memory 32*", "*decoder 33*", and "*D/A converter 34*" included in a plurality of "*column driver IC 14*") [figs. 1 and 3] coupled to the pixel electrodes, wherein the gray voltage generator generates gamma curves for different

pixel colors and selects gray voltages so that each of the data drivers determines a particular data signal for a particular pixel electrode by using one of the gray voltages [par. (0037)], the gray voltage generator including a first gamma voltage register which stores digital gamma voltages received from the signal controller ("*memory 32*") [fig. 3] [par. (0038) lines 1-2].

Park inherently teaches a common electrode and the liquid crystal layer being positioned between the pixel electrodes and the common electrode since it is required for any liquid crystal display to have a common electrode and to place the liquid crystal layer between the pixel electrodes and the common electrode, in order to control the liquid crystals of the layer by applying voltages between the pixel electrodes and the common electrode, and thus to display desired images based on the signals from the signal controller.

Park does not teach the gray voltage generator generating gray voltages that are each associated with a pixel color and the data driver determines a particular data signal for a particular pixel electrode by using one of the gray voltages that is associated with the pixel color of the particular pixel electrode.

However, Kudo teaches a concept of generating and processing different independent digital gamma signals for different pixel colors [par. (0107) lines 1-4 and par. (0108)].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the signal controller of Park to generate different independent digital gamma signals for different pixel colors by applying the concept of Kudo, i.e. generating different digital gamma signals for different pixel colors, to the apparatus of Park, and to modify the gray voltage generators of Park to produce analog gamma reference voltages that are specific to different pixel colors and are associated with the same pixel color as the image data, by including

additional memory, decoder, and D/A converter, by applying the concept of Kudo, i.e. processing different digital gamma signals for different pixel colors, to the apparatus of Park, in order to allow the data drivers of Park to output data voltages representing more accurate gamma curves to the liquid crystal panel of the display and thus to improve the image quality of the display.

Park as modified by Kudo teaches the plurality of data drivers being coupled to the plurality of gray voltage generator.

Park as modified by Kudo does not expressly teach the plurality of data drivers being coupled to a single gray voltage generator.

However, Nakano teaches a concept of including a single gray voltage generator ("*1436*") [fig. 14] coupled to a plurality of data drivers ("*source drivers 1435*") [fig. 14], which provides a plurality of reference voltages to the plurality of data drivers [col. 21 lines 42-49].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the apparatus of Park as modified by Kudo to include a single external gray voltage generator, instead of including a plurality of gray voltage generators, as taught by Nakano, in order to reduce the manufacturing cost of the liquid crystal display driving apparatus.

Park as modified by Kudo and Nakano teaches a first color-specific gamma voltage register (Park: a register included in "*memory 32*") [Park: fig. 3] storing digital gamma voltages received from the signal controller for a specific color.

Park as modified by Kudo and Nakano does not teach a second color-specific gamma voltage register coupled to the first color-specific gamma voltage register wherein the second

color-specific gamma voltage registers store digital gamma voltages received from the signal controller for a specific pixel color.

However, since the Applicant has failed to disclose having two color-specific gamma voltage registers instead of one color-specific gamma voltage register provides an advantage, is used for a particular purpose, or solves a state problem, it is an obvious matter of design choice to include two color-specific gamma voltage registers.

Furthermore, the courts have held that separating a single part (the color-specific gamma voltage register of Park as modified by Kudo and Nakano) into a plurality of separated parts (the first and the second color-specific gamma voltage register) is generally recognized as being within the level of ordinary skill in the art. *In re Dulberg*, 289 F.2d 522, 523, 129 USPQ 348, 349 (CCPA 1961).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use either one or two of color-specific gamma voltage registers to store digital gamma voltages received from the signal controller since either one or two of color-specific gamma voltage registers would perform equally well at storing digital gamma voltages temporarily.

As to **claim 13**, all of the claim limitations have already been discussed with respect to the rejection of claim 2.

As to **claim 15**, all of the claim limitations have already been discussed with respect to the rejection of claim 4.

As to **claim 16**, all of the claim limitations have already been discussed with respect to the rejection of claims 5 and 12.

As to **claim 17**, all of the claim limitations have already been discussed with respect to the rejection of claims 1 and 6.

As to **claim 19**, all of the claim limitations have already been discussed with respect to the rejection of claim 8.

As to **claim 21**, all of the claim limitations have already been discussed with respect to the rejection of claim 9.

4. **Claims 7** and **18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Park, Kudo, and Nakano as applied to claims 1, 2, 4-6, 8-9, 11-13, 15-17, 19, and 21 above, and further in view of Kitajima (US 5,091,722).

As to **claim 7**, Park as modified by Kudo and Nakano teaches the sampling unit (Park: a combination of "*D/A converter 28*" and "*buffer 30*" included in a plurality of "*column driver IC 14*") [Park: fig. 1] comprising a plurality of sampling circuits.

Park as modified by Kudo and Nakano does not expressly teach the structure of the sampling circuit.

However, Kitajima [fig. 13] teaches a sampling circuit ("*3*") included in a display apparatus, which comprises:

a switch ("*8*", "*9*", and "*10*") that turns on in response to a sampling signal from a signal controller;

a capacitor coupled to the switch for storing the sampled voltage data ("*17*", "*18*", and "*19*"); and

an analog buffer ("*20*", "*21*", and "*22*") coupled to the capacitor for outputting the stored voltage data.

It would have been obvious to one of ordinary skill in the art at the time of the invention to specify the structure of the sampling circuit of Park as modified by Kudo and Nakano to include a switch, a capacitor, and an analog buffer, as taught by Kitajima, in order to allow the display of Park as modified by Kudo and Nakano to sample the image data signals.

As to **claim 18**, all of the claim limitations have already been discussed with respect to the rejection of claim 7.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SEOKYUN MOON whose telephone number is (571)272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

November 26, 2008
/S. M./
Examiner, Art Unit 2629

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629